

CLAIMS

What is claimed is:

- 1           1.     An apparatus for allocating one or more resources to an instruction, the  
2     apparatus comprising:  
3           a sequence generator that generates one or more resource identifiers using at least a  
4     portion of a pseudorandom sequence, each resource identifier corresponding to one of the  
5     resources; and  
6           a resource identifier selector coupled to the sequence generator, the resource identifier  
7     selector selecting one or more of the resource identifiers for allocation to the instruction.

1           2.     The apparatus as recited in claim 1, wherein the resource identifier selector  
2 determines how many resource identifiers, if any, are required by the instruction based on an  
3 instruction requirements signal.

1           3.     The apparatus as recited in claim 1, further comprising a buffer including two  
2 or more buffer entries wherein each resource comprises one of the buffer entries.

1           4.     The apparatus as recited in claim 3, wherein the buffer comprises a reorder  
2 buffer.

1           5.     The apparatus as recited in claim 1, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison; and

6           a selector coupled to the one or more comparators and the resource identifier  
7 selection circuit.

1           6.     The apparatus as recited in claim 1, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison; and

6           a variable shifter coupled to the one or more comparators and the resource identifier  
7 selection circuit.

1           7.     The apparatus as recited in claim 1, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison;

6           a selector coupled to the one or more comparators and the resource identifier  
7 selection circuit; and

8           a highest identifier allocation circuit coupled to the selector.

1           8.     The apparatus as recited in claim 1, wherein the sequence generator further  
2 comprises:

3           a logic circuit coupled to the resource identifier selector; and

4           a storage array coupled to the logic circuit and the resource identifier selector.

1           9.     The apparatus as recited in claim 1, wherein the sequence generator further  
2 comprises a storage array coupled to the resource identifier selector.

          10.     The apparatus as recited in claim 1, wherein the sequence generator further  
comprises a logic circuit coupled to the resource identifier selector.

1           11.     The apparatus as recited in claim 1, further comprising an instruction decode  
2 unit and wherein the resource identifier selector generates a decoder stall signal issued to the  
3 instruction decode unit.

1           12.     The apparatus as recited in claim 1, wherein the portion of a pseudorandom  
2 sequence comprises a first resource identifier from within the pseudorandom sequence.

1           13.     The apparatus as recited in claim 12, wherein the resource identifier selection  
2 circuit comprises means for generating a second resource identifier from within the  
3 pseudorandom sequence based upon the first resource identifier.

1           14.     The apparatus as recited in claim 1, wherein the sequence generation circuit  
2 comprises a storage array and the portion of the pseudorandom sequence comprises a portion  
3 of each resource identifier within the pseudorandom sequence stored as elements within the  
4 storage array.

1           15.     The apparatus as recited in claim 14, wherein the portion of each resource  
2 identifier within the pseudorandom sequence comprises a least significant bit of each  
3 resource identifier within the pseudorandom sequence.

1           16.     The apparatus as recited in claim 14, wherein the resource identifier selection  
2 circuit comprises a variable shifter configured to shift elements of the storage array and the  
3 resource identifier selection circuit is configured to index the elements within the storage  
4 array.

1           17.     The apparatus as recited in claim 1, wherein the sequence generation circuit  
2 comprises a logic circuit and the portion of a pseudorandom sequence comprises a portion of  
3 each resource identifier within the pseudorandom sequence stored as elements within the  
4 storage array.

1           18.     The apparatus as recited in claim 17, wherein the portion of each resource  
2 identifier within the pseudorandom sequence comprises a least significant bit of each  
3 resource identifier within the pseudorandom sequence.

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1           19.    The apparatus as recited in claim 17, wherein the resource identifier selection  
2 circuit comprises a selector and a circuit to determine the highest identifier allocated  
3 configured to shift elements of the storage array and the resource identifier selection circuit is  
4 configured to index the elements within the storage array.

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selecting one or more of the resource identifiers for allocation to the instruction.

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1           21.           The method as recited in claim 20, further comprising the step of  
2 determining how many resource identifiers, if any, are required by the instruction based on  
3 an instruction requirements signal.

1           22.           The method as recited in claim 20, further comprising the step of  
2 comparing a selected resource identifier to an allocation bound and issuing a control signal in  
3 response to the comparison.

1           23.       The method recited in claim 20, wherein the portion of the pseudorandom  
2 sequence comprises a portion of each resource identifier within the pseudorandom sequence  
3 stored as elements within a storage array.

1           24.       The method as recited in claim 23, wherein the portion of each resource  
2 identifier within the pseudorandom sequence comprises a least significant bit of each  
3 resource identifier within the pseudorandom sequence.

1           25.       The method as recited in claim 20, further comprising:  
2 storing the portion of the pseudorandom sequence as elements within a storage array;  
3 and  
4 the selecting step comprises the steps of shifting the elements of the storage array and  
5 indexing the elements of the storage array in response to the shifting.

1           26.       The method as recited in claim 20, wherein the selecting step comprises the  
2 steps of:

3 identifying a most recently associated resource identifier from within the  
4 pseudorandom sequence; and

5 selecting a resource identifier from within the pseudorandom sequence based upon  
6 the most recently associated resource identifier.

1 27. The method as recited in claim 20, wherein the selecting step comprises the  
2 steps of:

3 determining a resource requirement of the instruction; and

4 associating the selected resource identifier with the instruction in response to the  
5 determination.

1 28. The method as recited in claim 20, wherein the selecting step comprises the  
2 steps of:

3 comparing the selected resource identifier to an allocation bound to determine  
4 whether a resource corresponding to the selected resource identifier is allocatable; and

5 associating the selected resource identifier with the instruction in response to the  
6 determination.

1 29. The method as recited in claim 28, further comprising the step of modifying  
2 the allocation bound in response to a deallocation of a resource.

1 30. The method as recited in claim 28, further comprising the step of generating  
2 an instruction decode stall signal in response to a determination that the resource  
3 corresponding to the selected resource identifier is not allocatable.



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1 31. A system comprising:

2 a memory storage device;

3 a bus coupled to the memory storage device;

4 a processor coupled to the bus, comprising a resource allocator for allocating one or  
5 more resources to an instruction; and

6 the resource allocator comprising:

7 a sequence generator that generates one or more resource identifiers using at  
8 least a portion of a pseudorandom sequence, each resource identifier corresponding to  
9 one of the resources; and

10 a resource identifier selector coupled to the sequence generator, the resource  
11 identifier selector selecting one or more of the resource identifiers for allocation to  
12 the instruction.

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1           32.     The system as recited in claim 31, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison; and

6           a selector coupled to the one or more comparators and the resource identifier  
7 selection circuit.

1           33.     The system as recited in claim 31, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison; and

6           a variable shifter coupled to the one or more comparators and the resource identifier  
7 selection circuit.

1           34.     The system as recited in claim 31, wherein the resource identifier selector  
2 further comprises:

3           one or more comparators coupled to the resource identifier selection circuit and  
4 configured to compare a selected resource identifier to an allocation bound and issue a  
5 control signal in response to the comparison;

6           a selector coupled to the one or more comparators and the resource identifier  
7 selection circuit; and

8           a highest identifier allocation circuit coupled to the selector.

1           35.     The system as recited in claim 31, wherein the sequence generator further  
2 comprises:

3           a logic circuit coupled to the resource identifier selector; and

4           a storage array coupled to the logic circuit and the resource identifier selector.

1           36.     The system as recited in claim 31, wherein the sequence generator further  
2 comprises a storage array coupled to the resource identifier selector.

1           37.     The system as recited in claim 31, wherein the sequence generator further  
2 comprises a logic circuit coupled to the resource identifier selector.